Transceiver with multi-state Direct Digital Synthesizer driven Phase Locked Loop

The invention relates to a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop.

The invention also relates to a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a phase locked loop for use in a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a digital synthesizer for use in a digital synthesizer driven phase locked loop for use in a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising said digital synthesizer driven phase locked loop, and to a system comprising at least one portable unit and at least one network unit for radio communication, with at least one unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a portable unit comprising a transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a network unit comprising at least one transceiver for transmitting signals in a transmitting mode and for receiving signals in a receiving mode and comprising a digital synthesizer driven phase locked loop, and to a method for transmitting signals in a transmitting mode and for receiving signals in a receiving mode via a digital synthesizer driven phase locked loop.

Such a transceiver is for example used in time division duplex (TDD) telecommunication systems or time division multiple access (TDMA) telecommunication systems, with said portable unit for example being a mobile phone and with said network unit for example being a base station or a router or a server etc.

Such a transceiver is known from US 5,859,570, which discloses a direct digital synthesizer (DDS) supplying a reference signal for a phase locked loop (PLL). According to this prior art, this DDS driven PLL uses a divided and frequency converted DDS signal as a reference for the PLL.

It is an object of the invention, inter alia, of providing a low cost transceiver as defined in the preamble.

The transceiver according to the invention is characterized in that said digital synthesizer driven phase locked loop, in said transmitting mode, is in a modulating state, with said digital synthesizer driven phase locked loop, in said receiving mode, being in an oscillating state.

By letting a transmitter part and a receiver part of said transceiver according to the invention share a single DDS driven PLL, which in said transmitting mode, is in a modulating state, and which in said receiving mode, is in an oscillating state (a frequency synthesizer state), a low cost transceiver has been provided.

The invention is based upon a basic idea, inter alia, of using important parts in low cost transceivers, having a transmitting mode and a receiving mode, for both modes, instead of using different parts for different modes.

The invention solves the problem, inter alia, of providing a low cost transceiver, which has a simple construction and nevertheless offers a good performance.

A first embodiment of the transceiver according to the invention as defined in claim 2 is advantageous in that said DDS receives, dependently upon the state in which it is, a modulation signal or a non-modulation signal, thereby avoiding any (state) switching inside the DDS.

A second embodiment of the transceiver according to the invention as defined in claim 3 is advantageous in that a low cost switch is used under control of a controller which for example comprises a mode detector for detecting a transmitting mode and a receiving mode and for example comprises a control signal generator for in response to said detecting generating said control signals. The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively.

A third embodiment of the transceiver according to the invention as defined in claim 4 is advantageous in that said PLL comprises, in said modulating state, a first filtering

performance allowing the generation of an improved modulated signal, with said PLL comprising, in said oscillating state, a second filtering performance allowing demodulation with reduced phase noise.

A fourth embodiment of the transceiver according to the invention as defined in claim 5 is advantageous in that said first filter for example being a loop filter and said second filter for example being a narrow band filter are being selected via a low cost switch. The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively.

A fifth embodiment of the transceiver according to the invention as defined in claim 6 is advantageous in that said PLL generates, dependently upon the state in which it is, a modulated signal destined for a transmitter part or a non-modulated signal destined for a non-transmitter part.

A sixth embodiment of the transceiver according to the invention as defined in claim 7 is advantageous in that low cost switches are used for supplying said modulated signal via said transmitter part to said antenna and for supplying said non-modulated signal to a demodulator for demodulating a radio signal received via said antenna and said receiver part. The transmitter part for example comprises an auto gain controller, a filter and a power amplifier. The receiver part for example comprises a filter, a low noise amplifier and an auto gain controller, with said demodulator for example working in a Zero Intermediate Frequency mode or a Near Zero Intermediate Frequency mode. The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively. Said demodulator and/or said receiver part together form said non-transmitter part.

Embodiments, of the digital synthesizer driven phase locked loop according to the invention, of the phase locked loop according to the invention, of the digital synthesizer according to the invention, of the system according to the invention, of the portable unit according to the invention, of the network unit according to the invention, and of the method according to the invention, correspond with the embodiments of the transceiver according to the invention.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments(s) described hereinafter.

Fig. 1 illustrates in block diagram form a transceiver according to the invention comprising a digital synthesizer driven phase locked loop according to the invention having a digital synthesizer according to the invention and a phase locked loop according to the invention.

Fig. 1 illustrates in block diagram form a transceiver according to the invention comprising a single direct digital synthesizer driven phase locked loop (DDS driven PLL) 24,10-15 according to the invention having a direct digital synthesizer (DDS) 24 according to the invention and a phase locked loop (PLL) 10-15 according to the invention. The transceiver comprises an antenna 1 coupled to an in/output of a switch 3 of which an input is coupled to an output of a transceiver part 2 and of which an output is coupled to an input of a receiver part 4. An input of transmitter part 2 is coupled to a first output of a switch 5, of which a second output is coupled to a first input of a demodulator 6 and of which an input is coupled to an output of PLL 10-15. A second input of demodulator 6 is coupled to an output of receiver part 4 and an output of demodulator 6 is coupled to an input of a controller 40.

PLL 10-15 comprises a voltage controlled oscillator (VCO) 10 of which an output forms the output of the PLL 10-15 and is further coupled to an input of a divider 15, of which an output is coupled to a first input of a phase detector 14. A second input of phase detector 14 is coupled to an output of DDS 24, and an output of phase detector 14 is coupled to inputs of two parallel filters 12,13, with an output of first filter 12 being coupled to a first input of a switch 11 and with an output of a second filter 13 being coupled to an second input of said switch 11. An output of switch 11 is coupled to an input of VCO 10.

DDS 24 comprises a filter 20 of which an output forms the output of DDS 24 and of which an input is coupled to an output of a D/A converter 21, of which an input is coupled to an output of a sine shaper 22 (like for example a ROM). An input of sine shaper 22 is coupled to an output of a phase accumulator 23. A clock input of DDS 24 is coupled via a multiplier 31 to a clock generator 30 and a signal input of DDS 24 is coupled to an output of a switch 32.

Controller 40 comprises a processor/memory system 42 coupled to the output of demodulator 6 and further coupled to a mode detector 41 (which possibly but not shown is further coupled to transmitter part 2 and/or receiver part 4 and/or demodulator 6) and to a control signal generator 43 and to a non-modulation signal generator 44 and to a modulation

signal generator 45. An output of modulation signal generator 45 is coupled to a first input of switch 32, and an output of non-modulation signal generator 44 is coupled to a second input of switch 32. An output of control signal generator 43 is coupled to control inputs of switches 11, 32, 3 and 5.

In time division telecommunication systems like time division duplex (TDD) telecommunication systems or time division multiple access (TDMA) telecommunication systems, during one or more first time slots, modulated signals are transmitted from the transceiver according to the invention to an other transceiver (transmitting mode), and during one or more second time slots, modulated signals are sent from the other transceiver to the transceiver according to the invention (receiving mode). According to prior art, a DDS driven PLL is used for generating a reference signal, like in US 5,859,570, which discloses a DDS driven PLL operating in a frequency synthesizing mode.

According to the invention - based upon a basic idea, inter alia, of using important parts in low cost transceivers, having a transmitting mode and a receiving mode, for both modes, instead of using different parts for different modes - said DDS driven PLL, in said transmitting mode, is in a modulating state, with said DDS driven PLL, in said receiving mode, being in an oscillating state.

Thereto, mode detector 41 detects the transceiver, during a first time-interval, being in a transmitting mode, for example via a coupling not shown to transmitter part 2, and/or for example by making a calculation, with said first and second time slots being standardized, and informs processor/memory system 42, which instructs modulation signal generator 45 to generate a modulation signal (for example in response to an audio signal originating from a man-machine-interface not shown and coupled to processor/memory 42) and instructs control signal generator 43 to generate a first control signal. In response to this first control signal, switch 32 supplies said modulation signal originating from modulation signal generator 45 to DDS 24, and switch 11 couples first filter 12 to VCO 10, with first filter 12 for example being a loop filter for improving the PLL function and for example having a bandwidth which is equal to or a little larger than the (occupied) bandwidth of the modulation signal. DDS 24 receives a multiplied clock signal comprising clock pulses via multiplier 31 and clock generator 30, and receives said modulation signal. At the hand of DDS 24, any signal including complex waveforms can be generated by defining one or more of at least three parameters being frequency, phase and amplitude respectively. These three parameters respectively can be controlled by frequency control words (with frequency modulation being achieved before/in phase accumulator 23), phase control words (with phase

modulation being achieved between/in phase accumulator 23 and sine shaper 22) and amplitude control words (with amplitude modulation being achieved between/in sine shaper 22 and D/A converter 21) respectively. Said modulation signal manipulates one or more of these control words, and as a result, DDS 24 generates a modulated reference signal which is supplied to PLL 10-15, which, via phase detector 14 and first filter 12 and switch 11 and VCO 10, with divider 15 being in a feedback loop, locks this modulated reference signal. The locked modulated reference signal is supplied via switch 5 to transmitter part 2, due to switch 5, for example in response to said first control signal or a further control signal originating from controller 40, connecting VCO 10 with transmitter part 2. Transmitter part 2, for example comprising an auto gain controller, a filter and a power amplifier, supplies an amplified, filtered and gain controlled locked modulated reference signal to switch 3 and therefore provides a direct digital RF modulation. Switch 3 supplies this signal to antenna 1, due to switch 3, for example in response to said first control signal or a further control signal originating from controller 40 via a coupling not shown, connecting transmitter part 2 with antenna 1. So, during this first time-interval, the transceiver is in a transmitting mode, and the DDS driven PLL 24,10-15 is in a modulating state.

Then, mode detector 41 detects the transceiver, during a second time-interval, being in a receiving mode, for example via a coupling not shown to receiver part 4, and/or for example by making a calculation, with said first and second time slots being standardized, and informs processor/memory system 42, which possibly instructs non-modulation signal generator 44 to generate a non-modulation signal (for example a dc-voltage adaptable via processor/memory system 42 or a ground voltage in which case said instructing does not necessarily have to take place) and instructs control signal generator 43 to generate a second control signal. In response to this second control signal, switch 32 supplies said non-modulation signal originating from non-modulation signal generator 44 to DDS 24, and switch 11 couples second filter 13 to VCO 10, with second filter 13 for example being a narrow band filter allowing demodulation with reduced phase noise. DDS 24 now generates a non-modulated reference signal (due to said non-modulation signal now not manipulating said control words but either supplying/defining predefined/fixed control words or not supplying/defining any control words at all in which case DDS 24 will use its own predefined/fixed values), which is supplied to PLL 10-15, which, via phase detector 14 and second filter 12 and switch 11 and VCO 10, with divider 15 being in a feedback loop, locks this non-modulated reference signal. The locked non-modulated reference signal is supplied via switch 5 to demodulator 6, due to switch 5, for example in response to said second

control signal or a further control signal originating from controller 40, connecting VCO 10 with demodulator 6. Receiver part 4, for example comprising a filter, a low noise amplifier and an auto gain controller, receives a (modulated) radio signal via antenna 1 and switch 3. Switch 3, for example in response to said second control signal or a further control signal originating from controller 40 via a coupling not shown, connects antenna 1 with receiver part 4, and supplies a gain controlled, amplified and filtered (modulated) radio signal to demodulator 6, which demodulates (for example via a Zero IF mode or Near Zero IF mode, which is very advantageous in that no expensive and bulky SAW IF filters are required) said last mentioned signal via said locked non-modulated reference signal. As a result, a demodulated signal is supplied to controller 40, for example via processor/memory system 42 to a man-machine-interface not shown which in response generates an audio signal. So, during this second time-interval, the transceiver is in a receiving mode, and the DDS driven PLL 24,10-15 is in an oscillating state.

By letting a transmitter part and a non-transmitter part (comprising a receiver part and/or a demodulator) of said transceiver according to the invention share a single DDS driven PLL, which in said transmitting mode, is in a modulating state, and which in said receiving mode, is in an oscillating state (a frequency synthesizer state), a low cost transceiver has been provided. Compared to prior art, like US 5,859,570 disclosing a DDS driven PLL always being in a frequency synthesizer state, the transceiver according to the invention is very advantageous, due to using said DDS driven PLL for different purposes. In other words, the transceiver is implemented using Radio Frequency direct modulation based on the DDS driven PLL and Radio Frequency demodulation (for example Zero IF, or Near Zero IF) based on the DDS driven PLL, which makes the transceiver low cost and small in size.

The invention solves the problem, inter alia, of providing a low cost transceiver (due to said transmitter part and said non-transmitter part - comprising said receiver part and/or said demodulator - sharing a single DDS driven PLL), which has a simple construction (by using one or more of said low cost switches) and nevertheless offers a good performance (due to the PLL dependently upon its mode using a specific mode-dependent filter). As a result, the transceiver according to the invention has a fast locking time in combination with less components, and therefore can have a smaller size and a lower weight.

Each block shown or not shown, can be 100% hardware, 100% software or a mixture of both. Each block shown or not shown can be integrated with each other block

shown and/or not shown. For example in controller 40, mode detector 41, control signal generator 43, non-modulation signal generator 44 and modulation signal generator 45 can be partly or entirely integrated with processor/memory system 42. Switch 32 can for example be located between DDS 24 and controller 40, or can for example form part of DDS 24 or controller 40 (in which case switch 32 can be partly or entirely integrated with processor/memory system 42). Switch 11 can for example form part of PLL 10-15, or can for example be located between PLL 10-15 and controller 40 (in which case filters 12,13 can for example be one or more filters which can be (de)activated and/or adjusted for providing first and second filtering performances), or can for example form part of controller 40 (in which case switch 32 can be partly or entirely integrated with processor/memory system 42, with filters 12,13 being one or more filters which can be (de)activated and/or adjusted for providing first and second filtering performances). Switch 32 can for example correspond with a demultiplexer, switch 11 can for example correspond with a selector or a multiplexer, switch 5 can for example correspond with a demultiplexer, and switch 3 can for example correspond with a multiplexer or a demultiplexer. Each switch can for example further correspond with a power divider. Sine shaper 22 and D/A converter 21 can for example also receive a clock signal, from clock generator 30 and/or multiplier 31.

The first control signal and the second control signal respectively may be completely different control signals or may be the same control signal having a first value and a second value respectively. Further, a third control signal etc. being a completely different control signal or being the same control signal having a third value etc. is not to be excluded, for example for creating a third mode, like a standby mode etc. So, the transceiver according to the invention comprises a multi-state (dual-state or more) DDS driven PLL.

In addition to said first and second filters 12,13, a third filter etc. is not to be excluded, for example for allowing different kinds of modulation signals to be dealt with differently in said PLL.

The fact that said DDS driven PLL, in said transmitting mode, is in a modulating state, implies that during at least a part of the first time-interval, said modulation signal is supplied to the DDS. And the fact that said DDS driven PLL, in said receiving mode, is in a non-modulation state, implies that during at least a part of the second time-interval, said non-modulation signal is supplied to the DDS. During a possible third time-interval, either said modulation signal or said non-modulation signal or a different signal or no signal at all may be supplied to said DDS.